2. **Listing of Items**
Applicant(s) sets forth below a list of all patents, publications or other information for consideration by the Office.

08/845,703

INFORMATION DISCLOSURE CITATION IN AN APPLICATION	Docket Number B-5500	Application Number ~~PENDING~~
	Applicant Ritu Shrivastava and Chitranjan N. Reddy	
	Filing Date	Group Art Unit N/A

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
SWC	5 5 5 2 3 3 1	9/3/96	Hsu et al.	437	40	7/11/95
	5 5 5 3 0 1 8	9/3/96	Wang et al.	365	185.01	6/7/95
	5 3 4 3 0 6 3	8/30/94	Yuan et al.	257	317	12/18/90
	5 2 9 2 6 8 1	3/8/94	Lee et al.	437	48	9/16/93
	4 8 6 8 6 1 9	9/19/89	Mukherjee et al.	365	185	11/21/84
	4 8 0 4 6 3 7	2/14/89	Smayling et al.	437	52	6/18/87
	5 0 7 7 6 9 1	12/31/91	Haddad et al.	365	218	10/23/89
SWC	5 2 6 2 6 6 2	11/16/93	Gonzalez et al	257	307	8/6/92

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (*Including Author, Title, Pertinent Pages, Etc.*)

SWC		Horiba et al., "A Symmetric Diagonal Driver Transistor SRAM Cell with Imbalance Suppression Technology for Stable Low Voltage Operation", IEEE Symposium on VLSI Technology 1996, pp. 144-145
SWC		Ohshima et al., "Process and Device Technologies For 16Mbit EPROMs With Large-Tilt-Angle Implanted P-pocket Cell", IEDM 1990, pp. 5.2.1 - 5.2.4

EXAMINER	DATE CONSIDERED
CRANE	9/28/98